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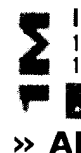
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## ASIC BIST synthesis: a VHDL approach

[Eberle, T.](#) [McVay, B.](#) [Meyers, C.](#) [Moore, J.](#)

DFT Technol. Group, Sanders Associates Inc., Nashua, USA;

*This paper appears in: Test Conference, 1996. Proceedings., International*

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### Abstract:

This paper describes the practical aspects of an automata design process and tool environment developed to rapidly effectively include **BIST** into ASIC designs. An overview **BIST** architecture is given describing **BIST** capabilities: mission logic, embedded and external **memory**, device interconnect **BIST** capability used to assist module/**BIST**. A high level synthesis approach is employed using VHDL language in a way unique to its intended purpose: automatic means for **instantiating** VHDL **BIST** structures.

an ASIC design is described. Other automated phases of development cycle are discussed including testability enhancement of the ASIC core and test stimulus generation. Foundry, factory, and field test. Results are presented for ASIC designs ranging in gate count from 56 k-164 k gates (complexity from controllers to data processors)

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